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Single Phase Fifteen Level Inverter using Seven Switches towards THD Reduction

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***Abstract*—** This paper proposes a single-phase fifteen-level inverter using seven switches, with a novel pulse width-modulated (PWM) control scheme. The Proposed multilevel inverter output voltage level increasing by using less number of switches driven by the multicarrier modulation techniques. The inverter is capable of producing fifteen levels of output-voltage (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage. A digital multi carrier PWM algorithm was implemented in a Spartan 3E FPGA. The proposed system was verified through simulation and implemented in a prototype.

***Keywords*—** Multilevel inverter; multi carrier modulation system; pulse width-modulation (PWM); total harmonic distortion (THD).

I. INTRODUCTION

Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, Output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of one novel modified H-bridge single-phase multilevel inverter that has one diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique.

II. MULTILEVEL INVERTER

Multilevel inverter is the generation of high voltage using lower voltage rating devices connected in series. Also it has the potential to get a high quality output voltage by producing multi output voltage levels. However it increases the number of switching devices and other components, which result in an increase of complexity problems and systems cost. Many multilevel inverter configurations have been researched to get a sinusoidal like output voltage wave with minimum circuit components. A multilevel inverter has several advantages over a conventional two level converter that uses high switching frequency pulse width modulation (PWM). The nice features of a multi level inverter can be briefly summarized as follows. Staircase waveform quality: Multilevel inverters not only can generate the output voltages with low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. Common mode voltage: Multilevel inverters produce small CM voltage, therefore the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore CM voltages can be eliminated by using advanced modulation technique. Input current: Multilevel inverters can draw input current with low distortion. Switching frequency: Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency means lower switching loss and higher efficiency. There are several multilevel converters are commercialized for high power applications such as Flexible AC transmission systems (FACTS) Controllers, HVDC, Train Traction, Automotive applications, renewable energy power conversion and transmission etc.

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase fifteen-level inverter was developed from the seven-level inverter. It comprises a Single phase conventional H-bridge inverter, three switches, and three voltage sources. This H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, for inverters of the same number of levels. Proper switching of the inverter can produce fifteen output-voltage levels (Vdc, 6Vdc/7, 5Vdc/7, 4Vdc/7, 3Vdc/7, 2Vdc/7, Vdc/7,0, -Vdc/7, -2Vdc/7, -3Vdc/7, - 4Vdc/7, -5Vdc/7, -6Vdc/7, -Vdc) from the dc supply voltage. The proposed inverter's operation can be divided into fifteen switching states, The required fifteen levels of output voltage were generated as follows.

1) Maximum positive output (*V*dc): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1, S2,S3 are ON the voltage applied to the load terminals is *V*dc.
2) 6/7 positive output (6*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S2,S3 are ON the voltage applied to the load terminals is 6*V*dc/7.
3) 5/7 Positive output (5*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1,S3 are ON the voltage applied to the load terminals is 5*V*dc/7.
4) .4/7 Positive output (4*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1 is

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ON and S2, S3 is OFF. The voltage applied to the load terminals is 4*V*dc/7.

5) 3/7Positive output (3*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S1 is OFF and S2, S3 is ON. The voltage applied to the load terminals is 3*V*dc/7.
6) 2/7 Positive output (2*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is 2*V*dc/7.
7) 1/7 Positive output (1*V*dc/7): *H*1 is ON, connecting the load positive terminal to *V*dc, and *H2* is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is 1*V*dc/7.
8) Zero output: All the switches S1, S2, S3, H1, H2, H3,H4 are in OFF position.
9) 1/7 Negative output (-1*V*dc/7): *H*3 is ON; connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is -1*V*dc/7.
10) 2/7 Negative output (-2*V*dc/7): *H3* is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is -2*V*dc/7.
11) 3/7 Negative output (-3*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S1 is OFF and S2, S3 is ON. The voltage applied to the load terminals is -3*V*dc/7.
12) 4/7 Negative output (-4*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is -4*V*dc/7.
13) 5/7 Negative output (-5*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground the switches S1,S3 are ON the voltage applied to the load terminals is -5*V*dc/7.
14) 6/7 Negative output (-6*V*dc/7): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S2,S3 are ON the voltage applied to the load terminals is –6*V*dc/7.
15) Maximum Negative output (-*V*dc): *H*3 is ON, connecting the load positive terminal to *V*dc, and *H4* is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is –*V*dc.

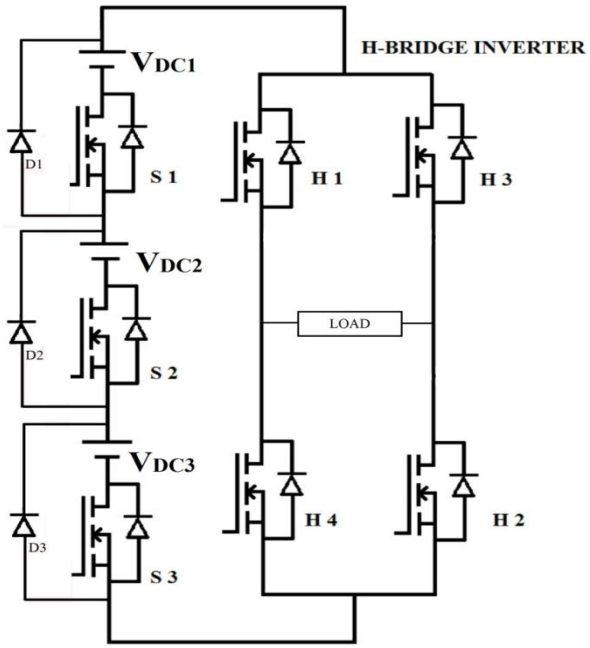

Fig. 1. Fifteen level inverter circuit diagram.

IV. PWM GENERATION

In this paper multi carrier pulse width modulation technique is used to generate the fifteen level output voltage. Seven equal amplitude carrier triangular signals with offset is compared with the sinusoidal reference signal. These PWM signals are given to the switches S1, S2, S3. Then the two sinusoidal signals having 180 degree displacement signals are compared with the carrier triangular signal, these PWM pulses are having dead band, it will avoid the shoot through problem between two devices. These PWM pulses are given to the single phase inverter circuit switches H1, H2, H3, and H4.

Voltage Level	S_3	S_2	S_1	H_1	H_2	H_3	H_4
V_{dc}	ON	ON	ON	ON	ON	OFF	OFF
$6/7V_{dc}$	ON	ON	OFF	ON	ON	OFF	OFF
$5/7\,V_{dc}$	ON	OFF	ON	ON	ON	OFF	OFF
$4/7\,V_{dc}$	ON	OFF	OFF	ON	ON	OFF	OFF
$3/7\,V_{dc}$	OFF	ON	ON	ON	ON	OFF	OFF
$2/7\,V_{dc}$	OFF	ON	OFF	ON	ON	OFF	OFF
$1/7\,V_{dc}$	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$-1/7\,V_{dc}$	OFF	OFF	ON	OFF	OFF	ON	ON
$-2/7\,V_{dc}$	OFF	ON	OFF	OFF	OFF	ON	ON
$-3/7\,V_{dc}$	OFF	ON	ON	OFF	OFF	ON	ON
$-4/7\,V_{dc}$	ON	OFF	OFF	OFF	OFF	ON	ON
$-5/7\,V_{dc}$	ON	OFF	ON	OFF	OFF	ON	ON
$-6/7V_{dc}$	ON	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}$	ON	ON	ON	OFF	OFF	ON	ON

Fig. 2. Switching sequence for 15 level inverter.

Here the switching device is MOSFET; as compared to IGBT the cost is low. The processor used here is FPGA (Field Programmable Gate Array). It's under the category of Very large scale integration system. In FPFA many of the pins are multiplexed pins. So we can use it as either input or output

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pins. The operating speed of the Spartan 3E controller operating speed is much greater than Digital signal processors. These controllers are used to generate the PWM pulses to the fifteen level inverter. The switching sequence for fifteen level inverter is shown in the table. The PWM pulses are generated using the FPGA Spartan 3E controller.

V. SIMULATION AND EXPERIMENTAL RESULTS

Matlab Simulink simulated the proposed configuration before it was physically implemented in a prototype.

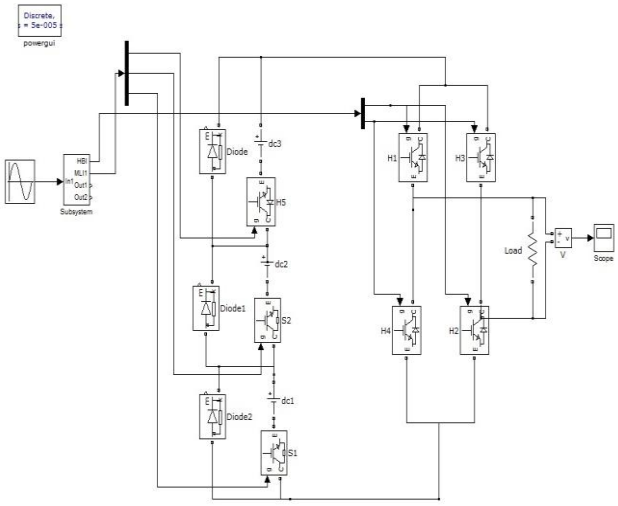

Fig. 3. Mat lab simulink model.

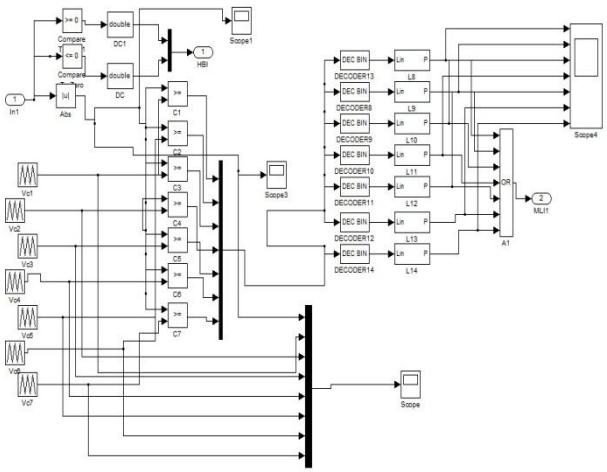

Fig. 4. Mat lab Simulink model for PWM generation.

The same amplitude with offset of seven carrier signal is compared with the sinusoidal reference signal and the PWM signal is generated.

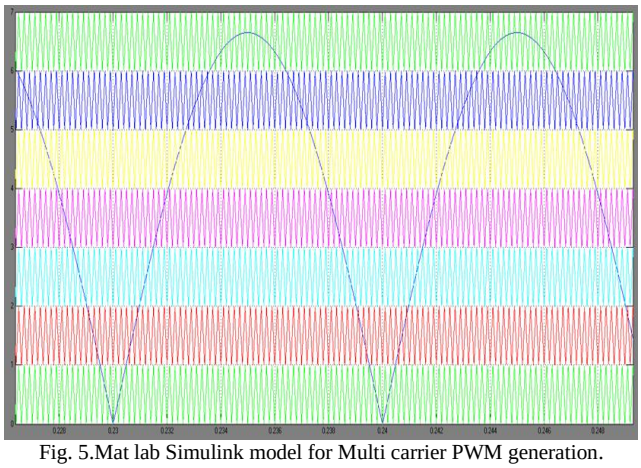

Fig. 5.Mat lab Simulink model for Multi carrier PWM generation.

The figure shows the thirteen level inverter output voltage, current by using Mat lab simulation.

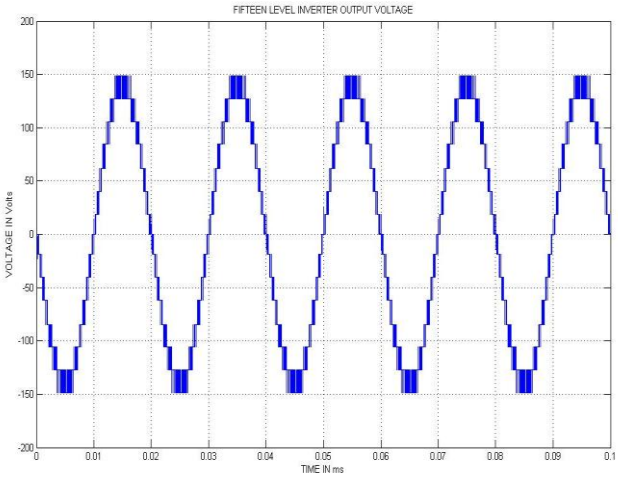

Fig. 6. Fifteen level inverter simulation output voltage.

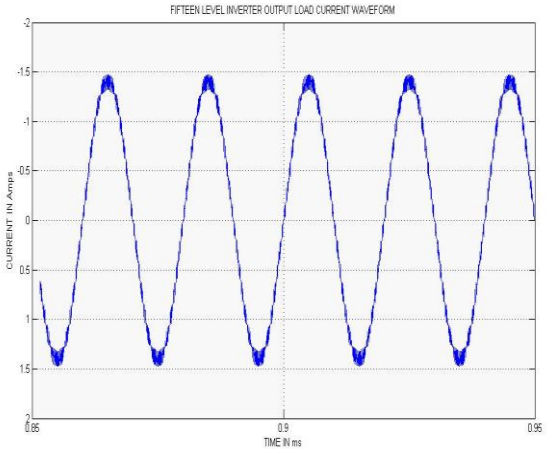

Fig. 7. Fifteen level inverter simulation output current.

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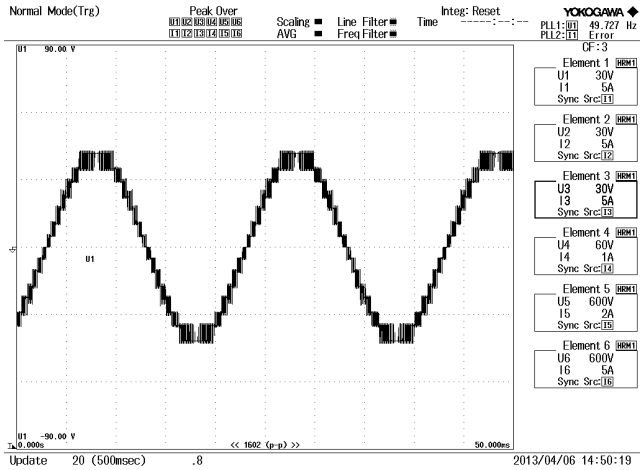

Fig. 8. Fifteen level inverter hardware output voltage.

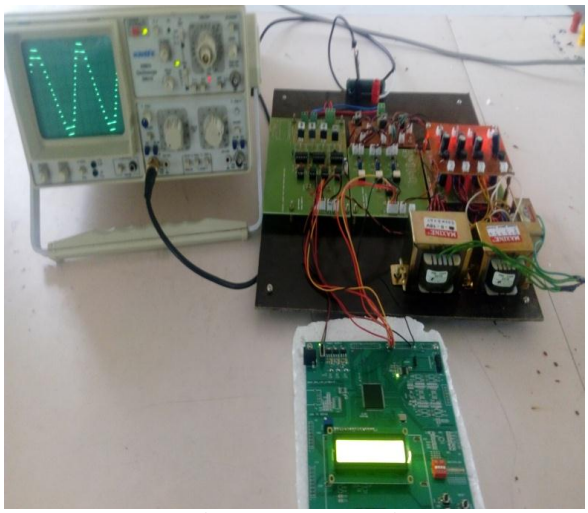

Fig. 9. Experimental setup for the single phase Fifteen levels PWM inverter.

VI. THD RESULT

By using YOKOGAWA the harmonics result is analysed.

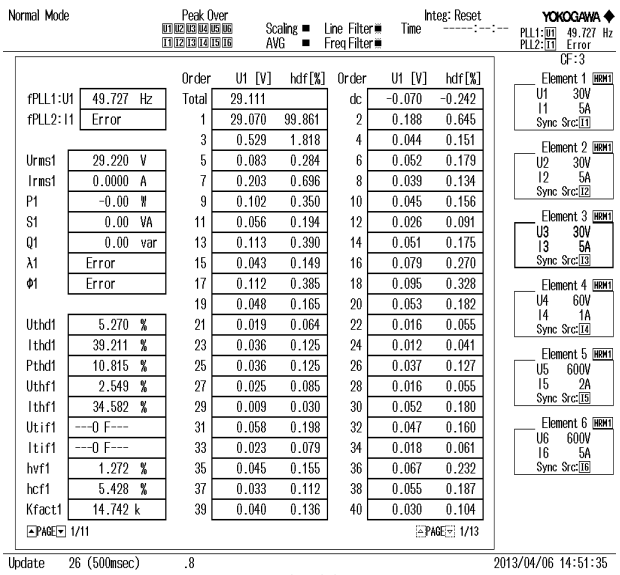

Fig. 10. THD Result for fifteen level inverter.

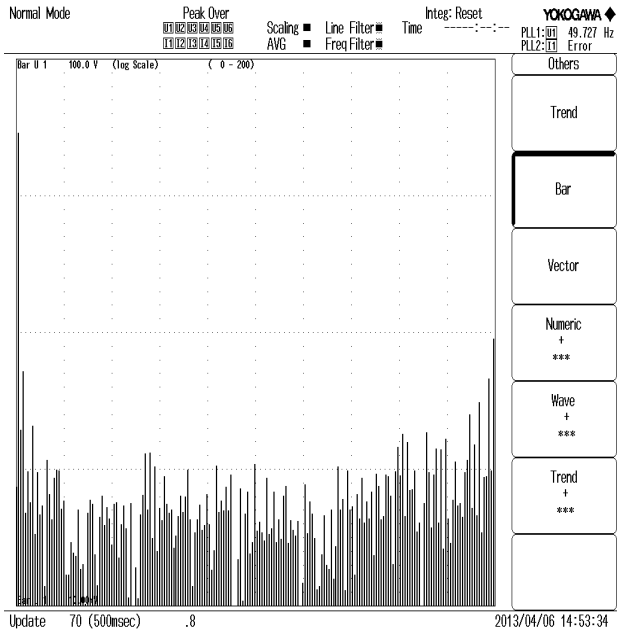

Fig. 11. THD bar chart for fifteen level inverter.

VII. THIRTEEN LEVEL OUTPUT VOLTAGE

By using the same hardware setup we can get the thirteen level output voltage. In multi carrier modulation technique six carrier signals are compared with the single reference signal is used to achieve the thirteen level output voltage. Proper switching of the inverter can produce thirteen output-voltage levels (Vdc, 5/6Vdc, 4/6Vdc, 3/6Vdc, 2/6Vdc, 1/6Vdc, 0, -5/6Vdc, -4/6Vdc, -3/6Vdc, -2/6Vdc, -1/6Vdc,-Vdc) from the dc supply voltage. A FPGA XILINS SPARTAN 3E is optimized the performance of the inverter. The THD level of this thirteen level inverter is 7.307 %.

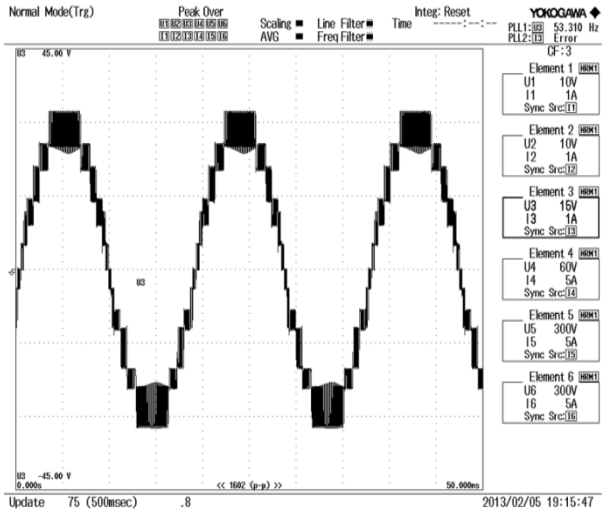

Fig. 12. Thirteen level inverter hardware output voltage.

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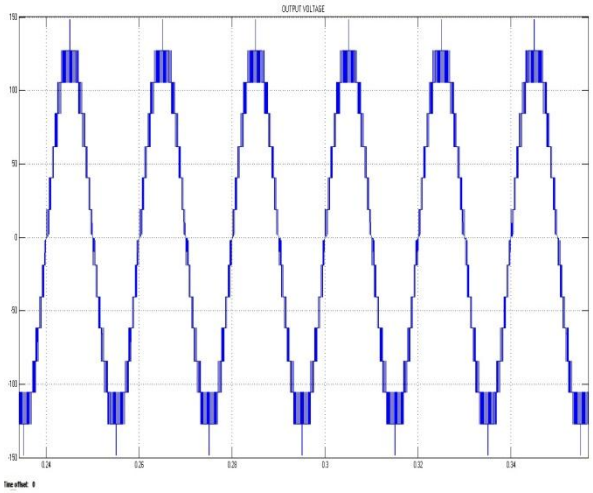

Fig. 13. Thirteen level inverter simulation output voltage.

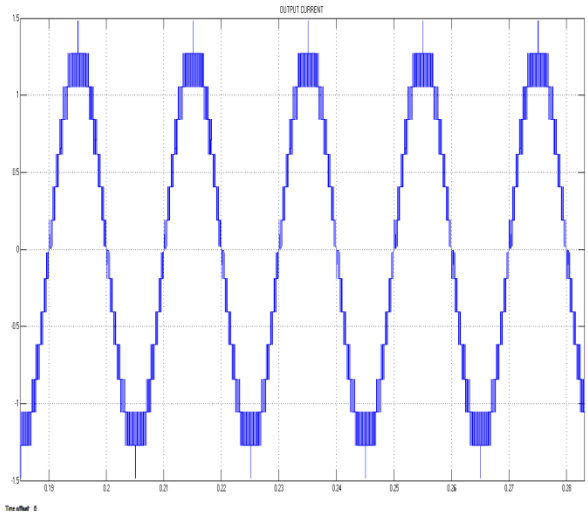

Fig 14. Thirteen level inverter simulation output current.

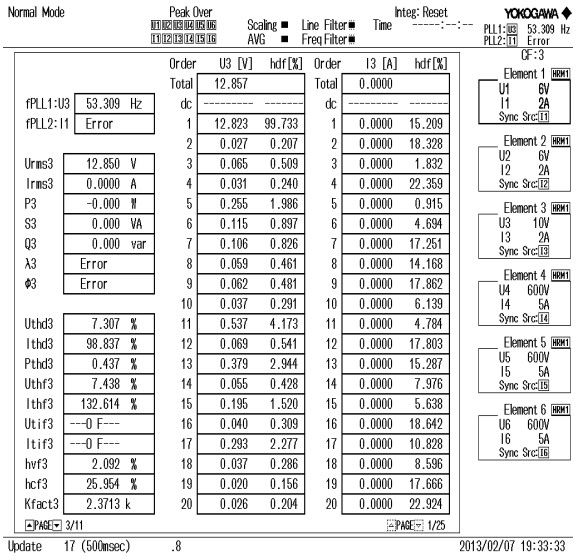

Fig. 15. THD Result for thirteen level Inverter.

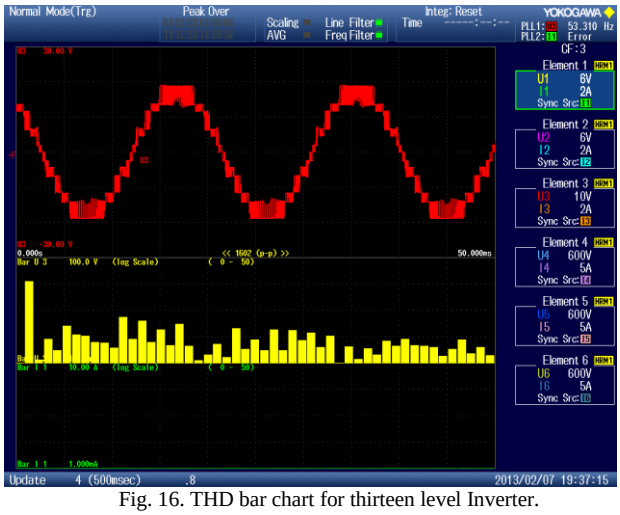

Fig. 16. THD bar chart for thirteen level Inverter.

VIII. CONCLUSIONS

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. In this paper only one reference signal and is compared with a triangular wave signal to generate the PWM signals. Here there are three different DC voltage levels are used in this multi level inverters. So this method of configuration is known as asymmetrical cascaded inverter. By controlling the modulation index and different levels of DC voltages the fifteen levels of the output voltage's achieved. A FPGA XILINS SPARTAN 3E is optimized the performance of the inverter. The THD level of this fifteen level inverter is 5.270 %.

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