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Heuristic Algorithms for Partitioning

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Abstract**—** In this paper partitioning algorithms are used to partition a large microelectronic system into smaller Application Specific Integrated Circuits (ASICS) as per the VLSI design flow requirements. Over the time, many of such algorithms have been evolved and still the work is in progress to make them more and more efficient in terms of area, propagation delay etc. Since most of the partitioning algorithms come under NP-complete set of mathematical problems, we use heuristic algorithms for these. This paper presents few of the heuristic algorithms and a comparison among them.

Keywords**—** Heuristic, Partitioning, ASIC, FPGA, K-L, Ratio, Algorithm

I. INTRODUCTION

The objectives of partitioning are:

a. Each ASIC having maximum size.
b. Maximum number of ASICs.
c. Each ASIC have maximum number of connections.
d. Total number of connections between them is maximum.

Every partitioning algorithm is supposed to fulfil above requirements and is mathematically evolved keeping in view the above objectives [6]-[10]. Some of the partitioning algorithms are: Kernighan-Lin (K-L), Fiduccia-Mattheyses (F-M), Ratio cut, simulated annealing, Look Ahead and so on [1]-[3], [11]-[12].

Section II describes K-L algorithm in detail. Section III gives review of some more partitioning algorithms. Section IV gives the comparison between the algorithms and Section V concludes the paper.

II. K-L ALGORITHM

A. Connectivity Measurement

Graph represents network, logic cells are represented by vertexes and electrical connections by edges as shown in figure 1. Net cuts appear when we divide the network into two giving net cutest while following same procedure for network graph gives edge cut and edge cutset. The number of net cuts and edge cuts are not necessarily equal as shown in figure 2.

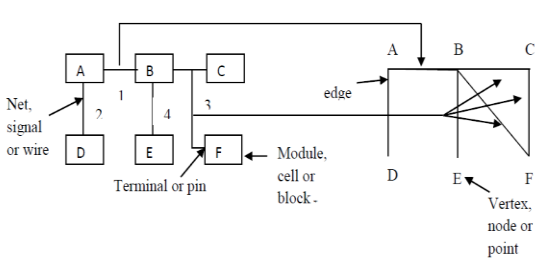

Figure 1. Graph of a Network

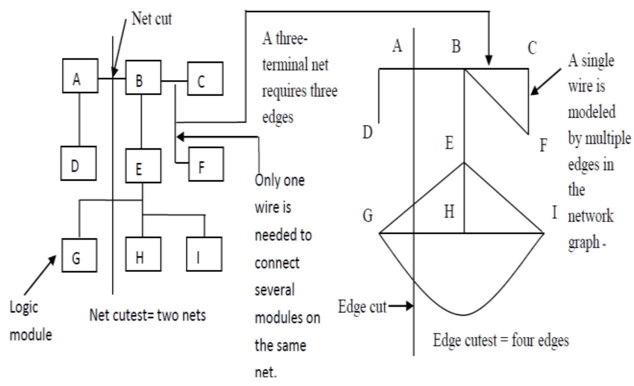

Figure 2. Edge Cutset and Net Cutset

B. K-L Algorithm Steps

Reducing the number of external connections is the objective of any partitioning algorithm. External connections are the connections between two ASICs. Firstly, connectivity matrix is defined C. Now, suppose we have a network with equal partitions A and B. Now we need to swap nodes between A and B so that cut weight W or external edge cost is minimum.

$$W = \sum_{a \in A,\, b \in B} C_{ab}. \qquad (1)$$

Consider graph and its partition as in figure 3 with W being 4.

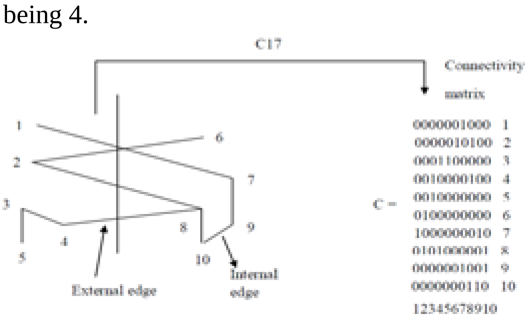

Figure 3. Connectivity matrix

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Steps for K-L algorithm are shown in Table I:

TABLE I. K-L Algo Steps

Steps	Description	Related Formula
1	Select two nodes a_i and b_i from A and B respectively that give maximum gain after swapping	$g_i = D_{ai} + D_{bi} - 2\, c_{ai\, bi.}$
2	Consider all the possible nodes a_i and b_i ; and pretend their swapping even if it gives zero or negative gain ; and then don't consider swapping those nodes again.	[No formula applicable in this step]
3	Repeat 1 and 2 until you have traversed all the nodes and encountered pretending all possible swaps. Now we have pair of nodes in A and B in order of the gain obtained via gain from interchanging those nodes.	[No formula applicable in this step]
4	Now the actual nodes to be swapped can be chosen. Consider first n nodes being swapped i.e X = $a_1, a_2, \ldots, a_n$ from A with Y= $b_1, b_2, \ldots, b_n$ nodes from B giving gain	$G_n = \sum_{i=1}^{n} g_i$
5	n is chosen corresponding to maximum value of G_n.	[No formula applicable in this step]

Check the value of G_n(max). If found to be greater than 0, swap X and Y and we will get cut weight reduced by G_n. If found equal to zero, then no improvement can be done.

III. Other Algorithms

A. *F-M Algorithm.*

The new features added in this as compared to K-L algorithm are:

a. Net-cuts costs reduction is the objective, cut size concept is given for hypergraphs.
b. Single move composes movement of single vertex.
c. Weighted vertices.
d. No need for balanced partition; introduces concept of balance factor for unbalanced patition.
e. O(p) time complexity, p being total terminals.

B. *Ratio Cut Algorithm*

Ratio cut is another partitioning approach used. It works on the following formula:

$$R = W / (A * B) \quad (2)$$

Where W= Cut Weight,
A= no. of cells in partition A
B= no. of cells in partition B

C. *Simulated Annealing Algorithm*

Simulated annealing is another probabilistic technique for partitioning. It is basically used when approximate solution will work rather than getting precise local solution. Annealing in metallurgy is the reason for its name. The working of algorithm is : During each step, a random solution which is close to the current one is selected by the algorithm. Then its quality is analyzed based on which decision is taken that whether we keep the new solution or remain with the previous one. It depends on whether the new solution is better or worse than the previous one. This is how we get a solution using this algorithm.

IV. Comparison Among Algorithms

Having studied few of the algorithmic techniques for partition, next step is to decide which algorithm is better as compared to other ones and how to decide onto which one to apply in which condition keeping in view the tradeoffs between them. Table II gives the comparison among various algorithms in terms of their complexity order and their main advantages.

TABLE II Comparison of different algorithms.

Year in which technique was proposed	Technique used for partitioning	Main advantages	Complexity order
1970	K-L algorithm	Reduction in Cut Weight	High
1982	F-M algorithm	Allow unbalanced partitions and extended to handle hypergraphs	High
1983	Simulated annealing	Flexible and able to approach global solution	High
1989	Ratio Cut algorithm	Removes restriction of constant partition sizes and partitions network into small highly connected groups	High

1991	Genetic algorithm	Always an answer and answer gets better with time.	Low
1998	Ratio Cut algorithm using hybrid genetic	Partitioning hypergraph into two disjoint groups of minimum cut ratio.	Low
2004	Ants optimization technique	Algorithm found best solution on small problem	low
2015	Improved adjacency matrix	Reduction in wire length and max cuts	low
2017	K-L algorithm using genetic implemented on MATLAB (proposed)	Reduction in cut weight and best solution obtained	Lowest

V. CONCLUSION

This paper gives a view of partitioning as main step in VLSI design flow; its requirement; objectives and scope. Next various algorithms that solve the partitioning problem as NP-complete mathematical problem i.e. Heuristic algorithms are discussed and their comparison is done on the basis of their complexity order and advantages keeping in view tradeoffs with area, effieciency etc.

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